ABSTRACT

A method of forming a double gated SOI channel transistor comprising the following steps. A substrate having an SOI structure formed thereover is provided. The SOI structure including a lower SOI silicon oxide layer and an upper SOI silicon layer. The SOI silicon layer is patterned to form a patterned silicon layer. A dummy layer is formed over the SOI silicon oxide layer and the patterned SOI silicon layer. The dummy layer is patterned to form a damascene opening therein exposing: a portion of the lower SOI silicon oxide layer; and a central portion of the patterned SOI silicon layer to define a source structure and a drain structure. Patterning the exposed lower SOI silicon oxide layer to form a recess. Gate oxide layer portions are formed around the exposed portion of the patterned SOI silicon layer. A planarized layer portion is formed within the final damascene opening. The planarized layer portion including a bottom gate and a top gate. The patterned dummy layer is removed to form the double gated SOI channel transistor.